GP 2133

In the United States Patent and Trademark Office

In re the application of
Lee D. Whetsel TI-31727

Serial No.: 09/955,542 Art Unit: 2133

Filed: 9/18/2001 Examiner: J. Kerveros

Title: Low Power Scan & Delay Test Method and Apparatus

Amendment A Under 37 CFR 1.111

July 29, 2004

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on July 29, 2004

Lawrence J. Bassuk, Reg. No. 29,043

Dear Sir:

Responsive to the Examiner's Action of 02/06/2004, please amend this application as follows:

In the Title:

Insert a new title as follows:

IC With Cache Bit Memory In Series With Scan Segment